PROSPECTS OF MICROSTRIP WAVEGUIDES IN ALUMINUM AND COPPER METALLIZATION FOR HIGH-FREQUENCY APPLICATIONS

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Abstract - An electrical characterization of the high-frequency behavior of monolithically integrated microstrip waveguides and a grounded coplanar line is presented. Microstrip lines fabricated with both aluminum metallization and copper metallization are compared in detail. Scaling laws and future metallization technologies are discussed. The waveguides are characterized by S-parameter measurements in a frequency range from 100 MHz to 80 GHz. After deembedding the characteristic impedance, propagation constant and telegraphers equation transmission parameter are extracted. Measurement results are compared to simulation results in detail. Advantages of aluminum and copper metallization are discussed.

Keywords: microstrip line, microwave guides, interconnect scaling, MMIC circuit design.

Resumo - Neste trabalho apresenta-se a caracterização elétrica do comportamento em altas freqüências de microlinhas e linhas coplanares aterradas, implementadas em tecnologia monolítica. Microlinhas fabricadas com metalização de alumínio e cobre são detalhadamente comparadas. As leis de escalonamento e as futuras tecnologias de metalização são discutidas. As linhas são caracterizadas através de medidas dos parâmetros S, na faixa de freqüência de 100 MHz a 80 GHz. Após a obtenção do valor da impedância característica, são extraídos a constante de propagação e os parâmetros da equação dos telegrafistas. Os resultados medidos são comparados com os resultados simulados. As vantagens das metalizações de alumínio e de cobre são discutidas.

Palavras-chave: Microlinhas, guias em microondas, escalonamento de interconexões, projeto de circuitos integrados monolíticos de microondas.

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1. INTRODUCTION

The success of the semiconductor industry is attributed to the advances in miniaturization. Due to the continuous shrinking of the minimum feature size, which is given by lithography limits, the devices are getting faster and faster. Compared to 1970 we can fabricate today 100 times smaller structures on the chip, where more than 20,000 times more transistors with faster switching times are integrated. Traditional scaling will probably no longer satisfy performance requirements. While technology scales down to nano-dimensions an ever increasing disparity between gate and wiring delay appears. The interconnect opportunities have to be considered for future integration.

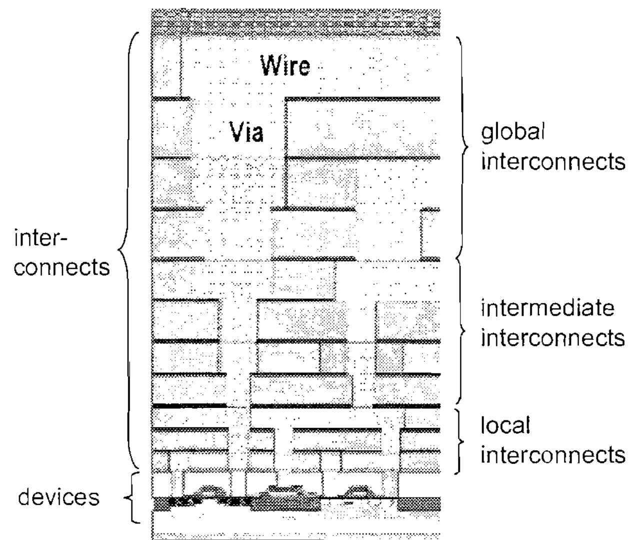

Figure 1. Cross-sectional sketch of hierarchical wiring system [1].

Nowadays silicon-based monolithic microwave integrated circuits tend to very high frequencies [2]. The designer has to pay attention to interconnect design, which influences the performance of ICs significantly [3]. Connections between circuit core and pads are long on-chip interconnects and in many cases realized as microstrip lines. The interconnect should meet many demands like low loss or to match a certain impedance.

Recent papers have presented several methods for characterizing transmission lines by the characteristic impedance [4, 5]. An ideal transmission line is completely characterized by the characteristic impedance Z_0 and the propagation constant γ. The characterization of the microstrip line is based on

Year of Production	2004	2007	2010	2013	2016
Technology node [nm]	90	65	45	32	22
Min. half pitch of local wires [nm]	105	75	52	37	25
Min. half pitch of intermediate wires [nm]	132	97	67	47	32
Min. half pitch of global wires [nm]	230	145	102	70	50
Total interconnect length [m/cm^2]	6880	11170	16060	22700	33510
Number of metal layers	9	10	10	11	11

Table 1. Interconnect technology requirements for next generation main processor units (MPUs) [1].

S-parameter measurement [6] with a thru-reflect-line (TRL) calibration [5, 7].

This paper shows an accurate characterization of monolithically integrated microstrip waveguides realized in copper and aluminum metallization and a coplanar waveguide up to 80 GHz. Section 2 shows modern metallization processes and the interconnect requirements addressed in the International Technology Roadmap for Semiconductors (ITRS). Scaling scenarios of interconnects are discussed in Section 3. Section 4 shows the differences between aluminum and copper metallization. In Section 5 the microstrip line geometries are described. For accurate measurement results in Section 6 the deembedding procedure is explained. Section 7 discusses the theory of S-parameter based transmission line characterization. In Section 8 the experimental results of the waveguides are presented and compared to simulation results in detail.

2. MULTILEVEL METALLIZATION

In next and over-next chip generations on-chip communication in terms of fast signal transmission within and between functional blocks is mainly determined by the interconnects or wiring systems. The basic functions of wires connecting the millions of transistors are the distribution of analog and digital signals as well as the distribution of power and supply voltage. For higher packing density and design flexibility the third dimension is used for interconnection. The resulting network of interconnects is called multilevel metallization, where metal interconnects span several layers isolated by the interlevel dielectric and connected vertically by vias (Fig. 1). According to the interconnect dimension the backend-of-line (BEOL) can be grouped into different types of wires. At local level short interconnects with minimum feature size are used to connect transistors. Intermediate wire dimensions are used for longer distances and wide interconnects with lengths up to 4 mm [8] are located at the upper or global level.

3. SCALING OF INTERCONNECTS

Global interconnects with large cross-sectional areas are mainly used, where high current densities and/or low resistances are needed. Due to the different scaling behavior of local and global interconnects the different levels of interconnects must be considered separately. Based on fundamental scaling laws assuming the same scaling factor $s < 1$ for all geometry dimensions the RC-delay of local wires remains constant for minimum feature sizes larger than 100 nm (Fig. 2(a)).

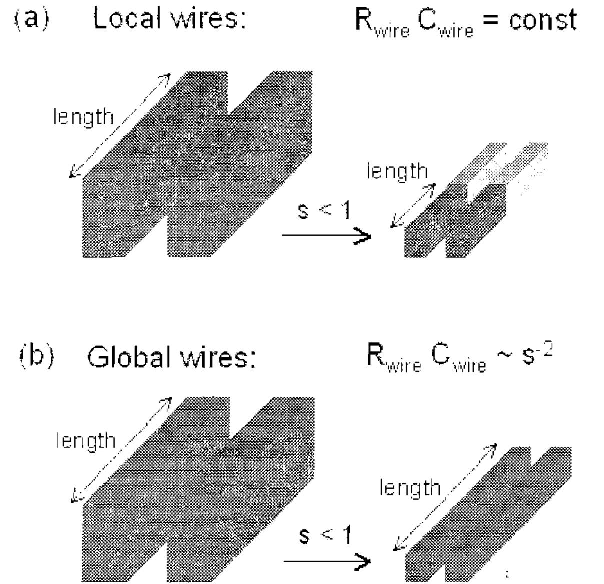

Figure 2. Scaling laws for local and global interconnects [9].

$$R_{wire}C_{wire} = const \quad (1)$$

For smaller wires, called nano-interconnects, the electrical size effect leading to increase in resistivity has to be taken into account [10]. The scaling scenario for global wires is slightly different. Due to the fact that global wires do not scale in length the wiring RC-delay of global wires scales with s^{-2}.

$$R_{wire}C_{wire} \sim s^{-2} \quad (2)$$

This is the dominant contribution to the overall signal delay time for long interconnections (Fig. 2(b)) [9]. Therefore advances in all disciplines of microelectronics are required to overcome this interconnect bottleneck and to guarantee highest chip performance for upcoming technologies. From the architecture perspective an aggressive hierarchical wiring system at the expense of additional wiring levels will be implemented in the BEOL in future chips [11]. This trend is also addressed in the International Technology Roadmap for Semiconductors (Fig. 1) [1]. The decreasing metal pitch and the increasing number of metal levels with increasing technology node are displayed in this roadmap (Tab. 1).

4. ALUMINUM AND COPPER METALLIZATION TECHNOLOGY

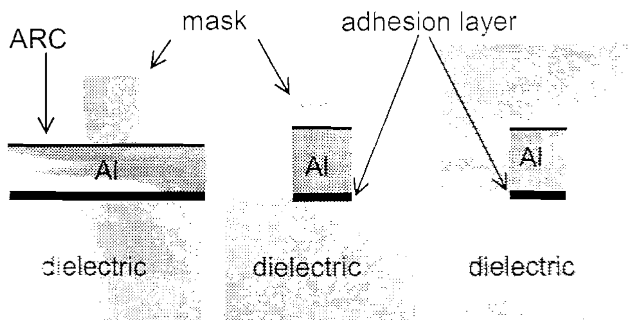

Figure 3. Subtractive Aluminum metallization technology.

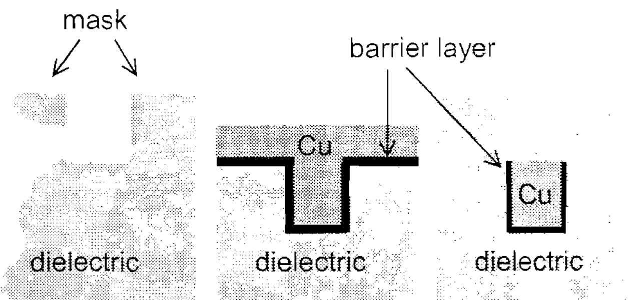

Figure 4. Copper Damascene process flow.

In order to investigate the high frequency behavior of global interconnects, microstrip lines fabricated in different metallization technologies are electrically characterized and compared. In recent years, aluminum was replaced by copper due to its higher conductivity resulting in less power required on chips and due to its better electromigration endurance. Conventionally, plasma etching was widely used for aluminum interconnect patterning. In this subtractive process aluminum is deposited as a blanket film on an adhesion layer; titanium nitride is usually used. For lithography reason an anti-reflecting coating (ARC) is deposited onto the aluminum layer followed by the metal etch through the mask. Finally the mask is removed to form the metal lines (Fig. 3).

With the introduction of copper, new integration schemes are necessary because no viable copper etch technology is currently available. To successfully integrate copper as material for interconnect applications the technology is shifting to damascene processing. In this in-laid technique, first trenches and/or vias are etched followed by the deposition of the metal stack including a barrier layer to prevent copper from diffusion into the dielectric and a seed layer acting as wetting layer for the subsequent electrochemical deposition. The metal excess is removed by chemical-mechanical polishing (Fig. 4). Due to different integration schemes the impact of the different barrier layers has to be considered. For the case of copper, which is a fast diffuser, barriers are needed at the trench bottom and on both sides of the trench. The barrier thickness will decrease with shrinking feature sizes in order to keep the ratio between copper and barrier area constant. In aluminum lines, which are not fully encapsulated, only a bottom titanium nitride is used for adhesion improvement. For an electrical assessment, high frequency measurements were applied to the microstrip lines based on both copper and aluminum metallization technology with silicon dioxide used as dielectric.

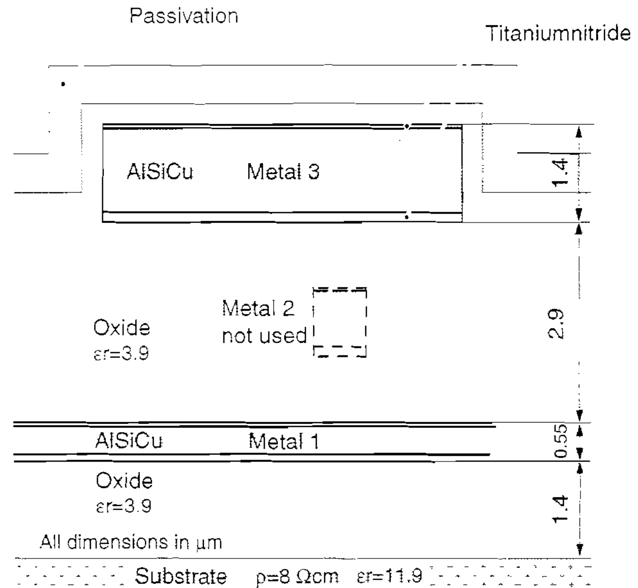

Figure 5. Detailed schematic cross section of the metallization.

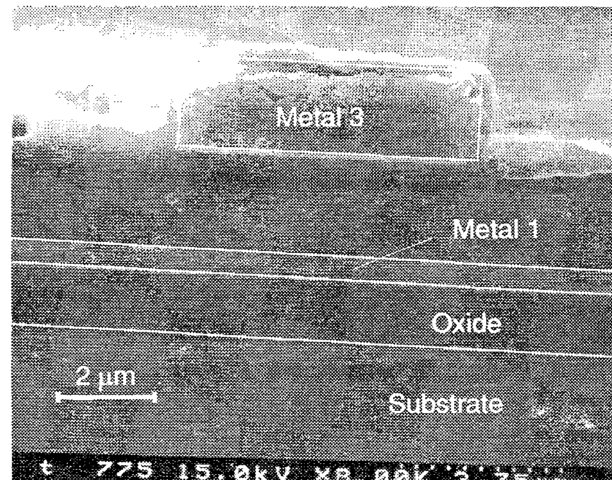

Figure 6. Cross section of the monolithically integrated microstrip line. Microstrip line is Metal 3. Ground Plane is Metal 1.

5. MICROSTRIP AND GROUNDED-COPLANAR LINE

We have measured and characterized three microstrip lines and a grounded-coplanar line. The grounded-coplanar line and two microstrip lines are realized in a copper metallization while one microstrip line is realized in a aluminum metallization.

5.1 MICROSTRIP LINE IN ALUMINUM

A detailed cross-section of the 3 layer aluminum metallization is shown in Fig. 5. The conductor material is standard AlSiCu and has a conductivity of $\sigma = 33\,\mathrm{S}/\mu\mathrm{m}$. The metal layers are embedded in silicon dioxide SiO_2 with a relative permittivity of $\varepsilon_r = 3.9$. The passivation is formed by a airproof protection coat and consists of silicon nitride Si_3N_4 and has an $\varepsilon_r = 7.5$. The substrate is a p^- doped Silicon with a conductivity of $\sigma = 12.5\,\mathrm{S/m}$ ($8\,\Omega\mathrm{cm}$). The upper metal (metal 3) is $1.4\,\mu\mathrm{m}$ thick.

The aluminum microstrip line is realized in Metal 3 as signal line and Metal 1 as ground plane. Metal 2 is not used. A cross-sectional micrograph of the microstrip waveguide is illustrated in Fig. 6. The microstrip line has a width of $w = 6\,\mu\mathrm{m}$ and a conductor-height of $T = 1.4\,\mu\mathrm{m}$ (Metal 3 in Fig. 5). The spacing between ground plane (Metal 1) and conductor is $H = 2.9\,\mu\mathrm{m}$. The width to height ratio of the microstrip is $W/H = 2.07$.

Fig. 7 shows the simulated electric field of the aluminum microstrip line. The lines of constant potential show that the most of the field energy is concentrated between line and ground plane. The lossy substrate is not penetrated by the field.

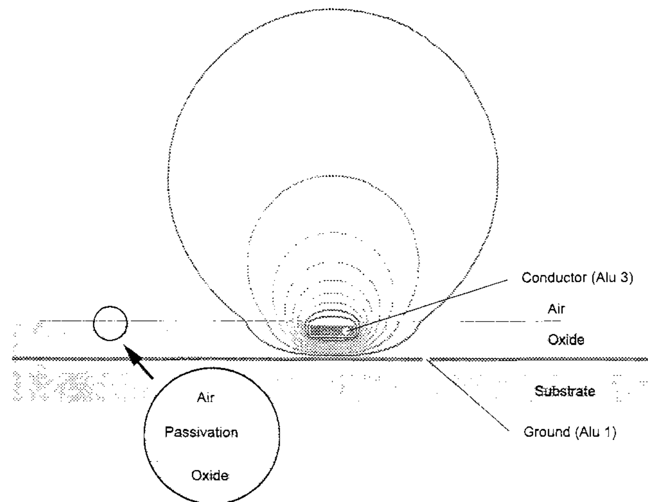

Figure 7. Simulated electric field (lines of constant potential) of the microstrip line.

5.2 MICROSTRIP LINE IN COPPER

The copper microstrip lines are realized in a $0.12\,\mu\mathrm{m}$ CMOS technology with six-layer copper metallization and silicon-oxide dielectric ($\varepsilon_r = 3.9$). Copper has a conductivity of $\sigma = 54\,\mathrm{S}/\mu\mathrm{m}$. The two topmost-layers are thick metals. The microstrip line again uses Metal 1 as ground plane. The signal lines are realized in Metal 6, which is a thick metal layer. Nevertheless, the thickness of Metal 6 of the copper process is about three times lower than Metal 3 in the aluminum process. As mentioned in Section 3 modern technologies have less metal thickness due to scaling. The microstrip lines in copper are realized in a similar way to the aluminum microstrip line (Fig. 5). The width to height ratio of the copper microstrip lines are $W/H = 1.44$ and $W/H = 1.80$.

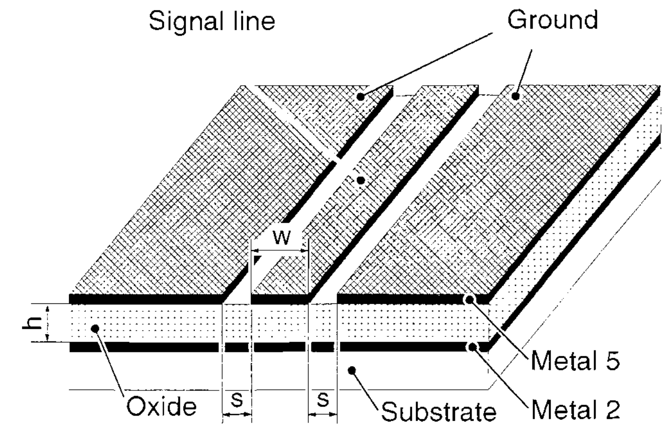

Figure 8. Schematic cross-section of a grounded-coplanar line.

5.3 GROUNDED-COPLANAR LINE IN COPPER

The grounded-coplanar line is realized in the same $0.12\,\mu\mathrm{m}$ CMOS technology with six-layer copper metallization. Without a ground plane the field of the coplanar line penetrates the substrate. This causes substrate loss and is highly undesirable. To overcome the substrate loss, a ground plane shields the field against the substrate. The ground planes left and right of the line and the line itself are realized in Metal 5. The ground plane under the line is realized in Metal 2. Fig. 8 shows a schematic cross-section of the grounded-coplanar line.

The width to spacing ratio of the grounded-coplanar line is $W/S = 7$. The width to height ratio of the ground plane to line is $W/H = 3.35$.

6. DEEMBEDDING

To extract the electrical characteristic of the waveguides from the measurement data, deembedding test structures are necessary. A calibration method with "short"and "open"test structures applies correct characterization only at low frequencies. To get accurate results at high frequencies up to 80 GHz, a thru-reflect-line (TRL) calibration is required. Fig. 9(a) shows a chip micrograph of the aluminum microstrip line test structure with $40\,\mu m$ high frequency pads on left and right side to interface with ground-signal-ground probes. The total length of the microstrip line test structure is $2800\,\mu m$. Fig. 9(b) shows the chip micrograph of the calibration test structure for deembedding.

If two-ports are connected in cascade the system can be practically defined by the transmission matrix (T-matrix). The measurement data are in the form of S-parameters and therefore we need the equations to get the T-matrix of a two-port.

$$\mathbf{T} = \frac{1}{S_{21}} \begin{pmatrix} 1 & -S_{22} \\ S_{11} & S \end{pmatrix} \quad (3)$$

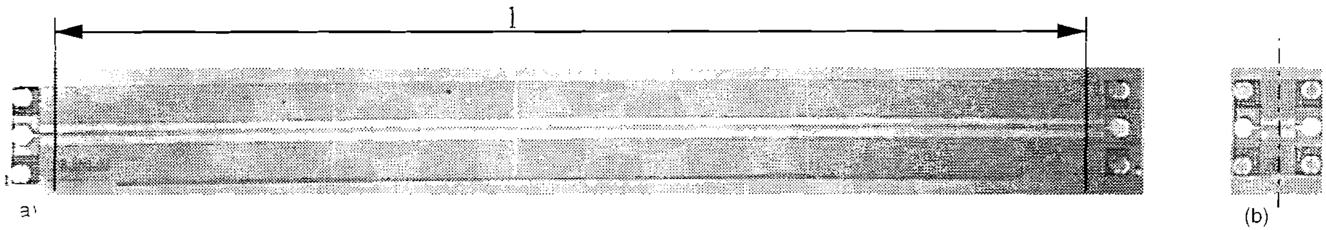

Figure 9. Chip micrograph high-frequency waveguide test structures. (a) Aluminum microstrip line test structure (l = 2500 μm). (b) Deembedding test structure.

where $S = \det(\mathbf{S}) = S_{11}S_{22} - S_{12}S_{21}$ is the determinant of the S-matrix. The T-matrix of the microstrip line test structure in Fig. 9(a) can be written as

$$\mathbf{T}_{Measure} = \mathbf{T}_{Pad_{left}} \cdot \mathbf{T}_{Line} \cdot \mathbf{T}_{Pad_{right}} \quad (4)$$

with T-matrix of the pads on the left and right side. On the other hand the T-matrix of the deembedding test structure in Fig. 9(b) can be written as

$$\begin{aligned} \mathbf{T}_{Pad} &= \mathbf{T}_{Pad_{left}} \cdot \mathbf{T}_{Pad_{right}} \\ \mathbf{T}_{Pad_{left}} &= \mathbf{T}_{Pad_{right}} = \sqrt{\mathbf{T}_{Pad}} \end{aligned} \quad (5)$$

From (4) and (5) we can extract the T-matrix of the microstrip line $\mathbf{T}_{Line}$ as follows

$$\mathbf{E} \cdot \mathbf{T}_{Line} \cdot \mathbf{E} = \mathbf{T}^{-1}_{Pad_{left}} \cdot \mathbf{T}_{Measure} \cdot \mathbf{T}^{-1}_{Pad_{right}} \quad (6)$$

where $\mathbf{E}$ is the unity matrix. After extracting $\mathbf{T}_{Line}$ we convert to the familiar S-parameter of the deembedded line.

$$\mathbf{S} = \frac{1}{T_{11}} \begin{pmatrix} T_{21} & T \\ 1 & -T_{12} \end{pmatrix} \quad (7)$$

where $T = \det(\mathbf{T})$.

7. PARAMETER EXTRACTION

After deembedding, we have extracted the S-parameters of the transmission lines, which describe the full electrical behavior. A figure of merit is the characteristic impedance Z and the propagation constant $\gamma = \alpha + j\beta$, where α is the attenuation constant and β is the phase constant. The S-parameter measured from a lossy unmatched transmission line with characteristic impedance Z and propagation constant γ in a Z_0 impedance system are [6]

$$\mathbf{S} = \frac{1}{D_s} \begin{pmatrix} (Z^2 - Z_0^2)\sinh\gamma l & 2ZZ_0 \\ 2ZZ_0 & (Z^2 - Z_0^2)\sinh\gamma l \end{pmatrix} \quad (8)$$

where $D_s = 2ZZ_0\cosh\gamma l + (Z^2 + Z_0^2)\sinh\gamma l$. The S-matrix can be solved in γ and Z. The product γl in terms of the S-parameter can be written as

$$\gamma l = -\ln\left(\frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm \sqrt{\frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2}}\right) \quad (9)$$

where l is the length of the deembedded line (Fig. 9). The characteristic impedance Z in terms of the S-parameter can be written as

$$Z = Z_0\sqrt{\frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2}} \quad (10)$$

The solutions of (9) and (10) must be chosen to be physically real.

A fundamental characteristic parameter of a waveguide is the attenuation constant α. It represents dielectric and ohmic losses of the waveguide. α can be calculated from (11) where γ was derived from (9).

$$\alpha = \mathrm{Re}\{\gamma\} \quad (11)$$

Not only the characteristic impedance and the propagation constant must be determined, but also the classical Telegraphers Equation transmission parameters (R, L, G and C) give a fundamental insight. These distributed circuit parameters describe per length unit and are not lumped element values. From the well known relation of a lossy transmission line

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (12)$$

$$Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (13)$$

we extract the Telegraphers Equation transmission parameters (R, L, G and C) as follows:

$$\begin{aligned} R &= \mathrm{Re}\{\gamma Z\} \\ L &= \mathrm{Im}\{\gamma Z\} \\ G &= \mathrm{Re}\{\gamma / Z\} \\ C &= \mathrm{Im}\{\gamma / Z\} \end{aligned} \quad (14)$$

8. EXPERIMENTAL RESULTS

The measurements are done on wafer-level with ground-signal-ground probes. The aluminum line is measured up to 80 GHz and the copper lines are measured up to 40 GHz. Additionally, the measurements of the aluminum line is compared to simulation results.

8.1 MEASUREMENT VERSUS SIMULATION

The aluminum microstrip line was designed to match 50 Ω. Fig. 10 shows measured and simulated characteristic impedance Z versus frequency. The unsteady peak at 50 GHz is due to the different measurement setup in the range from 50 MHz to 50 GHz and from 50 GHz to 80 GHz.

The characteristic impedance Z is separated into the absolute value (Fig. 10) and the phase (Fig. 11) as a function of

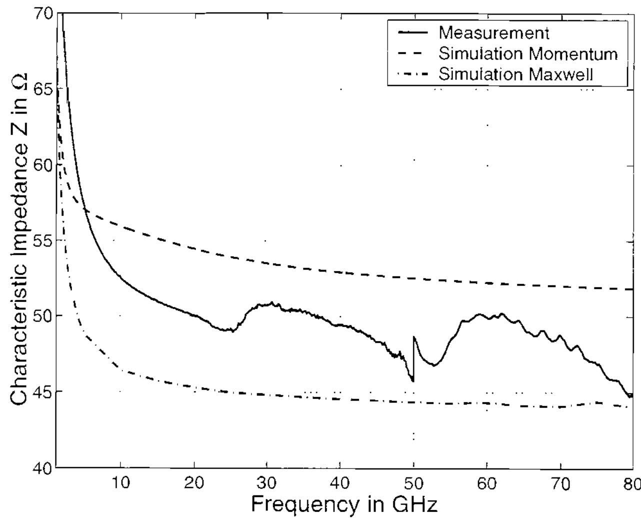

Figure 10. Measured and simulated characteristic impedance versus frequency of the $W/H = 6\,\mu\text{m}/2.9\,\mu\text{m}$ aluminum microstrip line.

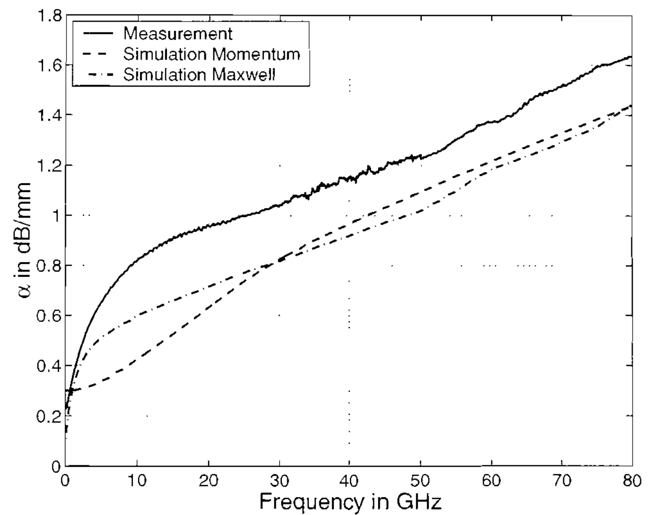

Figure 12. Measured and simulated attenuation per mm versus frequency of the $W/H = 6\,\mu\text{m}/2.9\,\mu\text{m}$ aluminum microstrip line.

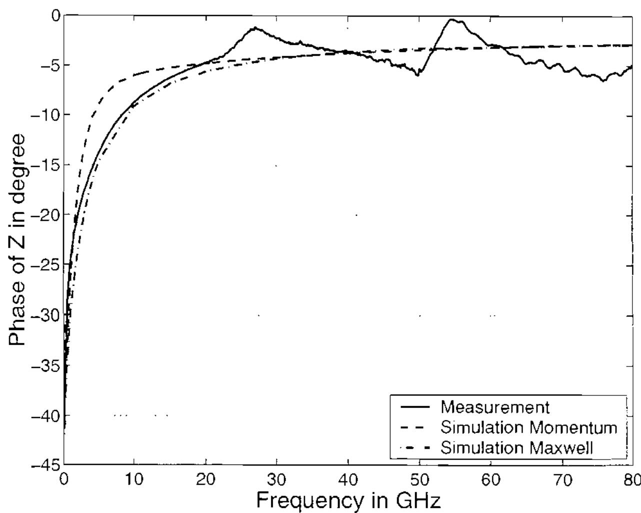

Figure 11. Measured and simulated phase of the characteristic impedance versus frequency.

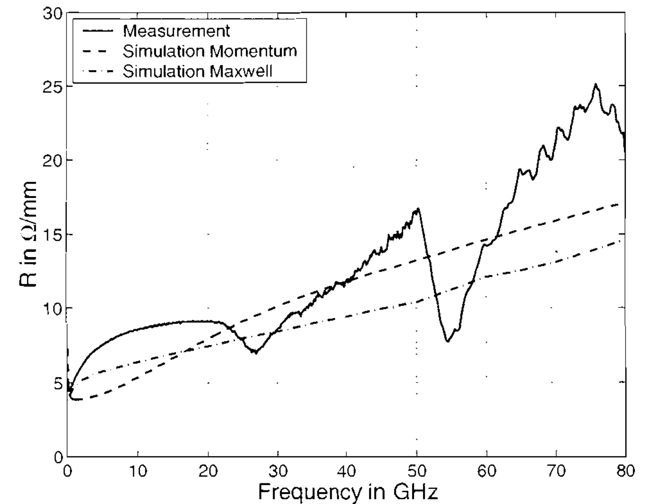

Figure 13. Measured and simulated characteristic series resistance versus frequency. The calculated series resistance of 3.8 Ω/mm matches the measurement at low frequencies.

frequency. At frequencies lower than 15 GHz the magnetic- and electric-field are not in phase (-40° at 50 MHz) and the microstrip line carries a slow wave mode. At high frequencies, the microstrip line exhibits a quasi-TEM mode.

At frequencies where the microstrip line length is a multiple of the half wave length, the S-parameter measurement is very sensitive [12]. In our case this effect causes measurement errors at 27 GHz and 54 GHz. At these frequencies, the extracted characteristic impedance Z, the characteristic series resistance R and the characteristic capacitance C are strongly influenced due to the measurement errors.

Fig. 12 shows the measured attenuation compared to simulations with Maxwell Field Simulator [13] and Momentum Field Simulator [14]. The small deviation between measurement and simulation validates the parameter extraction from the S-parameter measurement. As expected, the attenuation constant α increases with frequency. The increasing attenuation can be explained by the skin effect and the polarization losses of the dielectric.

Fig. 13 shows the measured and simulated characteristic series resistance slightly increasing with frequency. The calculated series resistance of 3.8 Ω/mm matches the measurement at low frequencies. The skin-depth at 20 GHz is 0.6 μm which is about a half of the conductor height T. The series resistance is very sensitive to measurement errors of the phase of Z.

The characteristic conductance is very sensitive to measurement errors of the phase of Z. The values of the characteristic conductance over frequency is in the same range as the measurement error and therefore has not been illustrated.

Fig. 14 illustrates the measured and simulated characteristic inductance versus frequency of the microstrip line. The inductance is slightly decreasing from DC up to 10 GHz due to the current crowding in the conductor. At frequencies higher

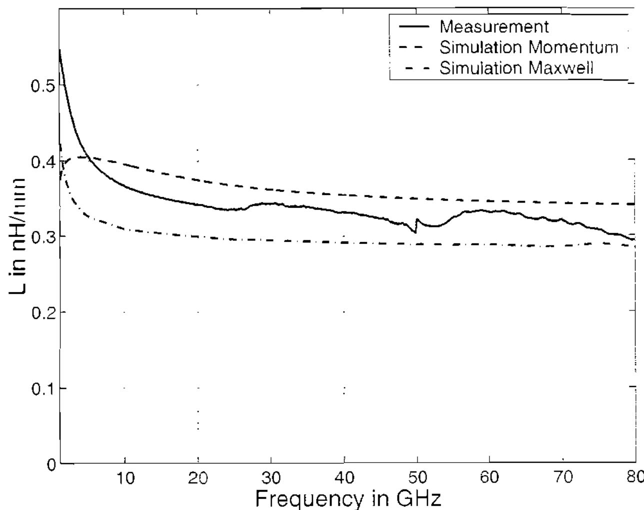

Figure 14. Measured and simulated characteristic inductance versus frequency of the $W/H = 6\,\mu m/2.9\,\mu m$ microstrip line.

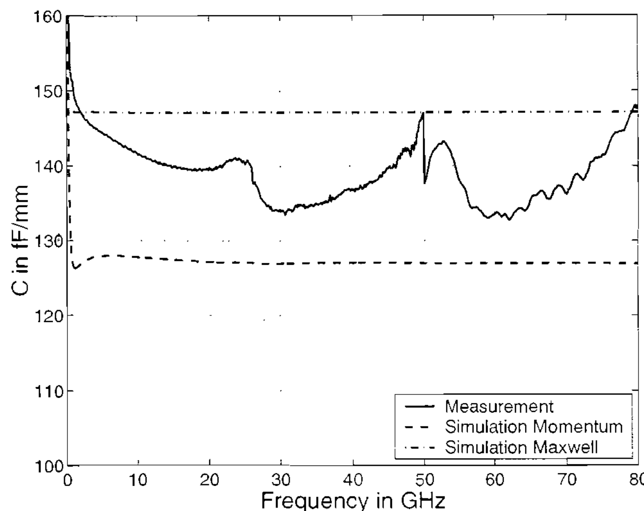

Figure 15. Measured and simulated characteristic capacitance versus frequency of the $W/H = 6\,\mu m/2.9\,\mu m$ microstrip line.

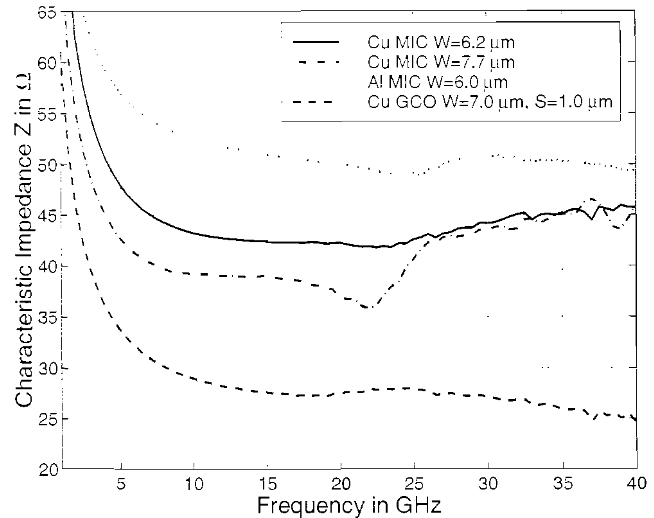

Figure 16. Measured characteristic impedance versus frequency of the microstrip and grounded coplanar lines.

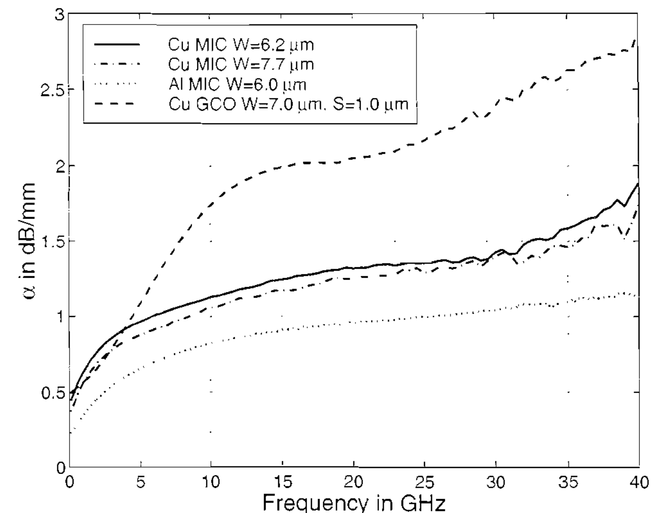

Figure 17. Measured attenuation per mm versus frequency of the copper microstrip and grounded coplanar line.

than 10 GHz the inductance is relatively constant.

The characteristic capacitance plot in Fig. 15 shows a high capacitance at low frequencies and a relatively constant capacitance at frequencies higher than 10 GHz. The capacitance from DC to 10 GHz is reduced because the propagation mode changes from a slow wave mode to a quasi-TEM mode.

8.2 ALUMINUM LINE VERSUS COPPER LINE

More and more aluminum has been replaced by copper metallization. Copper has a much higher conductivity compared to aluminum. Nevertheless, modern technologies have less metal thickness due to scaling (Section 3). We have realized microstrip lines in aluminum and copper to compare the electrical behavior.

Fig. 16 shows measured characteristic impedance Z versus frequency. The aluminum microstrip line (Al MIC) meets $50\,\Omega$ exactly. The copper microstrip lines (Cu MIC) have characteristic impedance lower than $50\,\Omega$. Copper fill structures have higher characteristic capacitance and therefore lower impedance. The copper microstrip line with a width $W = 6.2\,\mu m$ has a characteristic impedance of $43\,\Omega$ while the other copper line ($W = 7.7\,\mu m$) has a $Z = 38\,\Omega$. The grounded-coplanar line (Cu GCO) has a low impedance $Z = 28\,\Omega$ due to the copper fill structures, which are necessary for achieving good chemical-mechanical polishing (CMP) homogenities. On the other hand the impedance of coplanar lines is very sensitive to the spacing S (Fig. 8). This implies the need of a stable and accurate metallization process.

One of the most important parameters of a waveguide is the attenuation α. Fig. 17 shows the measured attenuation α of the waveguides. The two copper microstrip lines have nearly the same attenuation of about 1.7 dB/mm. As not expected, the aluminum microstrip line has less attenuation than the copper lines. However, it must be reminded that the thickness

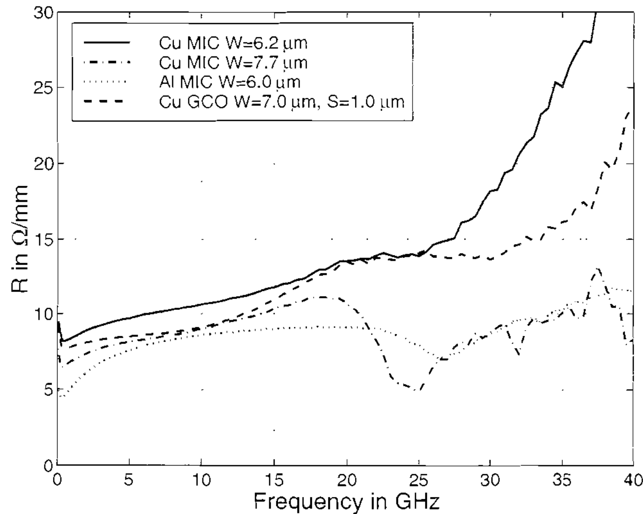

Figure 18. Measured characteristic series resistance versus frequency.

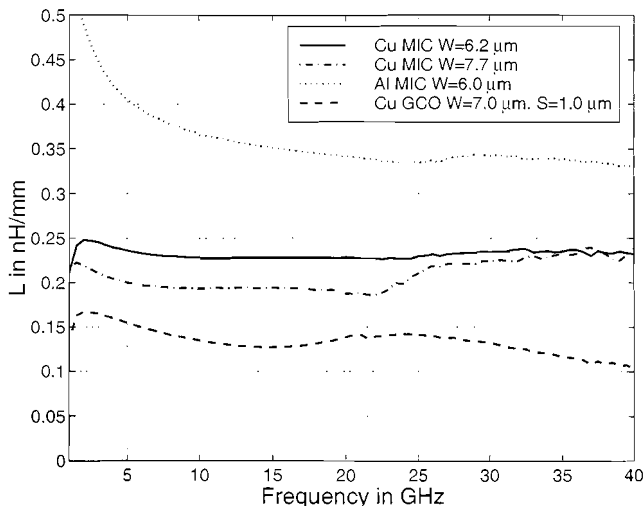

Figure 19. Measured characteristic inductance versus frequency of the copper microstrip and grounded coplanar line.

of Metal 6 of the copper process is about three times lower than Metal 3 in the aluminum process. The scaling laws of equation (2) effect the attenuation of the copper lines. Low attenuation implies the need of hierarchical metallization in future process technologies (Section 2).

The skin effect is more relevant on copper lines than on aluminum lines. The skin-depth at 30 GHz in copper is $0.4\,\mu$m and in aluminum $0.54\,\mu$m. This is already the size of about a half of the conductor height T. The full advantage of copper with its high conductivity is not valid any longer at very high frequencies.

Fig. 18 shows the measured characteristic series resistance of the lines. Again, the copper lines have a higher resistance than the aluminum line due to the smaller metal thickness. The skin-effect already starts at 30 GHz at the copper lines.

The characteristic conductance is very sensitive to measurement errors of the phase of Z. The values of the characteristic conductance over frequency is in the same range as

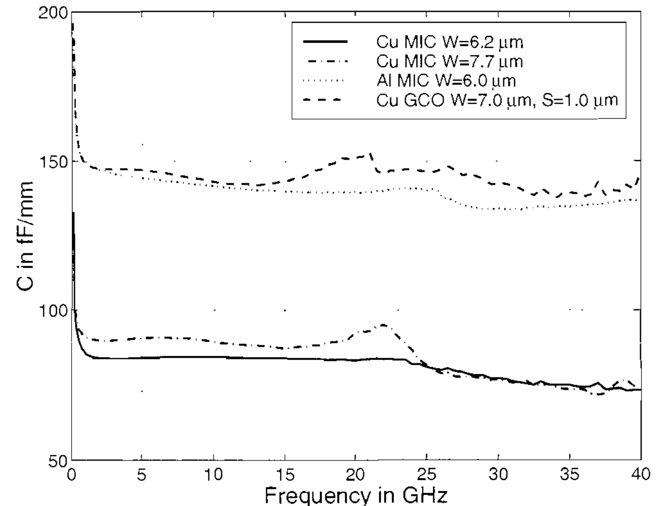

Figure 20. Measured characteristic capacitance versus frequency of the copper microstrip and grounded coplanar line.

the measurement error and therefore has not been illustrated.

Fig. 19 illustrates the measured characteristic inductance versus frequency of the waveguides. The inductance is nearly constant over the whole measured frequency range for all waveguides.

The characteristic capacitance plot in Fig. 20 shows a nearly constant capacitance for all realized waveguides. The dielectric of the copper metallization and the aluminum metallization is the same (silicon-oxide, $\varepsilon_r = 3.9$). The greater distance of the copper microstrip lines to the ground plane produces a lower capacitance than on the aluminum microstrip line. The capacitance of the grounded-coplanar line is mainly determined by the spacing S.

9. CONCLUSION

In recent years, aluminum was replaced by copper due to its higher current carrying capability resulting in less power required on chips and due to its better electromigration endurance. On the other hand, continuous shrinking, which is determined by lithography limits, leads to thinner metal layers which have more resistance. We have shown that a copper microstrip line does not have necessarily less attenuation than an aluminum line. In next and over-next chip generations it is highly desirable to have a hierachical metallization available. Thick top metals are necessary to get less attenuation for global interconnects. Thin bottom metals are necessary to connect the millions of transistors. An accurate characterization of waveguides on silicon up to 80 GHz was presented. With the deembeding algorithm, the electrical behavior of the waveguides can be extracted. The characteristic impedance, propagation constant and telegraphers equation transmission parameter of the waveguides give a fundamental insight of its performance.

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